5

## ABSTRACT OF THE DISCLOSURE

A test circuit disposed between a common bus and the cores of a multi-core computer permits post-silicon validation in the form of controlled stress testing of the system. The test circuit may block data requests from one or more selected cores and issue test data requests into the system instead, resulting in a more controllable test environment. In one embodiment, the test circuit is programmed and monitored from an external device through an integrated test port.